

### **REMARKS**

In response to the Office Action mailed March 27, 2003, Applicant respectfully requests reconsideration. To further the prosecution of this application, each of the issues raised in the Office Action are addressed herein. Claims 1-5 have been examined. By this amendment, claim 4 has been amended and new claims 6-16 have been added. Accordingly, claims 1-16 are pending in this application, of which claims 1, 4 and 6 are independent claims.

#### **I. Objections to the Specification**

The Office Action objects to the specification for the use of the unit ohms/square (i.e., ohms-per-square). However, ohms/square is the proper unit of measurement involving surface resistivity in connection with thin layers. The resistance of a thin layer or film is dictated by its geometry and the particular resistivity of the material forming the film. In particular, the resistance may be expressed as  $R = (\rho/d) (l/w)$  where  $\rho$  is the specific resistivity of the material,  $d$  is the thickness,  $l$  is the length, and  $w$  is the width of the layer of material.

The ratio  $\rho/d$  is often referred to as the sheet resistance and is measured in ohms. Whenever the length is equal to the width (i.e.,  $R$  is measured over a square), the second parenthetical term  $(l/w)$  in the expression above becomes unity and its dimensional units cancel regardless of magnitude (i.e., regardless of whether the units of length and width were in cm., inches, feet, etc.). As such, the units of the entire expression become ohms-per-square or ohms/square. That is, each square of material having a resistivity  $\rho$  and thickness  $d$  will exhibit the same resistance whether it be a square foot or a square centimeter.

Ohms/square is the widely accepted unit of measurement for the resistance of thin layers and would have been known and understood by those skilled in the art at the time of the invention. Accordingly, Applicant respectfully requests that the objection be withdrawn.

Additionally, the Examiner objects to the term "volume breakdown" and requests that the word volume be replaced by voltage. However, the term "volume breakdown" refers to a specific breakdown of a PN junction. For example, in the device shown in Fig. 3C, there are generally two regions susceptible to breakdown between the emitter region 24 and the base region 23. The first region includes the PN junction at the bottom side of region 24 (i.e., the generally horizontal PN junction between emitter region 24 and base region 23). The second

region includes the PN junction near the surface on the lateral sides of region 24 (i.e., the generally vertical PN junction between emitter region 24 and base region 23).

In a vertical transistor, the breakdown of the generally horizontal PN junction typically results in a breakdown in volume of the base region. That is, the volume of base material (e.g., base region 23) between the emitter and the collector undergoes avalanche breakdown to produce voltage-current characteristics as described in the specification. However, a breakdown near the surface of the generally vertical PN junction may not cause the base region to break down in volume, which as Applicant notes on page 4 lines 20-22, may not provide the intended satisfactory effects.

In the embodiment illustrated in Fig. 4B, for example, the lightly doped N-ring 27 is provided to ensure that breakdown occurs in volume in the desired region. Accordingly, the term "volume breakdown" is appropriate and correct and Applicant respectfully requests that the Examiner withdraw the objection.

## II. Objections to the Claims

The Examiner objects to the use of the units "ohms/square" recited in claim 2. As discussed above, the unit "ohms/square" is the proper unit of measurement for resistances of thin layers or films. Accordingly, it is respectfully requested that the objection be withdrawn.

In addition, the Examiner objects to the language "breakdown occurs in volume" as recited in claim 3. As discussed above, the term volume breakdown or a breakdown in volume is proper. As such, it is respectfully requested that the objection be withdrawn.

## III. Claim Rejections Under 35 U.S.C. § 103

In the Office Action, claims 1, 2, 3 and 5 are rejected under 35 U.S.C. § 103(a) as allegedly being obvious over Rault (U.S. Patent No. 5,751,531) in view of Ishii et al (U.S. Patent No. 4,405,932) and Williams et al (U.S. Patent No. 5,374,843). This rejection is respectfully traversed.

### A. There is No Motivation to Combine Rault and Ishii

The Office Action concedes that Rault does not discuss a transistor operating as a diode with open base and grounded collector. However, the Office Action asserts that Ishii "discloses an NPN transistor with grounded collector and open base and discusses the collector-emitter

breakdown voltage with the open base resulting in a negative resistance characteristic.” The Office Action asserts that it would have been obvious to one having ordinary skill in the art at the time of the invention to have modified Rault by Ishii “to use a transistor in this configuration as a diode because this is how diode junctions are formed.” Applicant respectfully disagrees.

In particular, that transistors and diodes both are comprised of PN junctions is insufficient motivation and does not suggest or explain why one skilled in the art would be motivated to modify the clipping device of Rault by incorporating the teaching of the reference diode of Ishii. The two references are directed to entirely different devices, and more importantly, have entirely different operating characteristics.

The clipping device of Rault is designed to break down according to the avalanche effect to protect against overvoltages on the order of 1000 volts by conducting currents on the order of 40A (*see e.g.*, col. 3, lines 33-45 of Rault). In contrast, the reference diode of Ishii is designed to break down according to the punch-through effect to regulate a reference voltage on the order of 6V by conducting currents during breakdown on the order of several pA to several mA (*see e.g.*, col. 1, lines 59-62 of Ishii). These two devices operate on entirely different scales to achieve entirely different results.

Rault discloses a clipping device for absorbing electrical overvoltages and Ishii discloses a reference diode for maintaining a reference voltage. The considerations for each respective device, particularly with respect to the operating conditions and characteristics, are far different and not applicable to each other. First, the two devices do not even share a common breakdown phenomenon of the PN junction. Rault relies on the avalanche effect, while Ishii describes a reference diode that breaks down according to the punch-through effect. This difference in breakdown phenomenon is due in part to the radically different conditions under which the devices operate and the different results the devices are intended to achieve.

In particular, the Rault device considers I-V characteristics three orders of magnitude greater in voltage and at least three orders of magnitude greater in current than the Ishii device. For example, the Ishii reference is directed to providing a constant voltage characteristic for currents in the pA to mA range. These considerations simply have no bearing on a clipping device designed to absorb 1000V, 40A surges. In fact, the Ishii device would not perform or function as described within the operating ranges of Rault. As such, the Ishii reference simply is

not applicable to Rault, nor are the two respective devices or the teachings thereof in any way compatible.

Accordingly, one skilled in the art would not be motivated to modify the high voltage, large current clipping device of Rault with the reference diode of Ishii having features adapted to maintain voltage characteristics at an entirely different (by three or more orders of magnitude) scale. The purported combination is therefore improper and should be withdrawn.

B. Ishii Teaches Away From the Purported Modification to Rault

Not only would one skilled in the art not have been motivated to make the purported modification, but Ishii specifically teaches away from devices having characteristics of the claimed invention. In particular, Ishii teaches away from transistor arrangements having open bases precisely because they exhibit negative dynamic resistance.

The excerpt of the Ishii reference relied on by the Office Action (i.e., col. 5, lines 29-48) describes the characteristics of transistors in general when the base is not shorted to the collector and is set forth by Ishii precisely to illustrate undesirable arrangements. That is, the transistor having an unconnected base and a voltage applied to the emitter is precisely what the Ishii reference teaches against. This is evidenced particularly in the paragraph beginning at col. 5, line 48 (i.e., the paragraph following the paragraph relied on by the Office Action), which states in relevant part:

On the other hand, in the punch-through reference diode according to this invention, the base and collector are shorted, so that the transistor action, i.e., the current amplification does not take place. Accordingly, even when the current  $I_{CEO}$  flows, it is not amplified, and any fluctuation of the current gain  $h_{fe}$  ascribable thereto does not occur, either. This prevents the voltage  $V_{CEO}$  from fluctuating and therefore prevents the negative resistance from occurring. Thus, the occurrence of the negative resistance is perfectly prevented, whereby abrupt constant-voltage characteristics can be attained. (emphasis added).

The Office Action relies on material in Ishii that is set forth merely as a description of what not to do. It is not a teaching but rather a teaching away. As such, this is an improper basis for a rejection. In the final paragraph of §2141.02, the MPEP states that “[a] prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention.” The thrust of Ishii is to provide a reference diode that avoids

the characteristics of the transistor described in the paragraph drawn upon by the Office Action to establish the rejection. Accordingly, one skilled in the art would not have been motivated to combine Rault with Ishii and would in fact have been led away from making the modification alleged in the Office Action. The combination of Rault with Ishii is therefore improper for this additional reason.

C. The Combination of Rault and Williams is Improper

The Office Action concedes that Rault and Ishii do not disclose a vertical transistor. However, the Office Action asserts that Williams discloses “the use of thicker epitaxial layers for providing a vertical NPN transistor” and that it would have been obvious to one of ordinary skill in the art at the time of the invention to “have modified Rault by Williams et al to increased [sic] the epitaxial layers in thickness because this is how higher breakdown voltages are obtained.” Applicant respectfully disagrees.

First, as best as can be understood by Applicant, the rejection set forth in the Office Action does not even purport to modify Rault by a vertical transistor at all. Rather, the Office Action purports to modify Rault with the “thicker epitaxial layers” of Williams. However, one does not obtain a vertical transistor merely by adding a thick epitaxial layer to the Zener diode of Rault (or even the planar transistor of Ishii). Accordingly, the purported modification set forth in the Office Action fails even to cure the conceded deficiencies of Rault and Ishii (i.e., the purported modification does not provide a vertical transistor).

In addition, the purported motivation for modifying Rault with the thicker epitaxial layer of Williams is alleged to be “because this is how higher breakdown voltages are obtained.” However, the clipping device of Rault does not suffer from low breakdown voltages. In fact, the Rault device is designed to handle voltages in the same range (e.g., 1000 volts) as the epitaxial layers of Williams (e.g., see col. 3, lines 35-45 of Rault). Nowhere is it suggested that higher breakdown voltages are desirable, nor is that an attribute sought by Rault or by the present invention. In fact, the purported modification would not even have the effect of increasing the breakdown voltage.

It should be appreciated that the present invention contemplates clipping devices having breakdown voltages significantly reduced from the Rault device (e.g., approximately in the 10-20 volt range as shown in FIGS. 5 and 6 and described on page 5, line 13 *et. seq.*). Accordingly, one skilled in the art would not be motivated to provide a thick epitaxial layer in Rault to

increase the breakdown voltage of the clipping device, when such a characteristic is simply not desired. As such, in addition to failing to provide the missing vertical transistor, the addition of the epitaxial layer is entirely lacking in motivation.

Assuming, *arguendo*, that the rejection set forth in the Office Action intends to modify Rault by the vertical transistor mentioned in Williams, it should be appreciated that Williams is directed to lateral DMOS transistors, not vertical transistors (see col. 3 line 48 *et. seq.*, col. 5 line 54 *et seq.*, etc.). Williams provides an epitaxial layer to improve the breakdown characteristics of a lateral LDD DMOS and notes that the epitaxial layer incorporated into the design of the lateral transistor may be used for “other purposes” such as providing a vertical NPN transistor.

However, Williams does not indicate anything about the structure of the vertical transistor and is completely silent with respect to fabrication, operation or use of vertical transistors. In fact, Williams is directed entirely to subject matter other than vertical transistors. The Office Action does not mention how the zener diode of Rault (not to mention the zener diode of Rault as modified by the planar transistor of Ishii) may be modified by Williams to arrive at the claimed invention (e.g., a clipping device having, *inter alia*, a vertical NPN transistor). Williams nowhere mentions either clipping devices, reference diodes or anything related to the Rault or Ishii disclosures. The Office Action fails to suggest (or even allege) why the mere mention of an epitaxial layer formed for an entirely different purpose (in a disclosure unrelated to clipping devices) that may also be used to form in part a vertical transistor would motivate one skilled in the art to modify Rault (or even Ishii) in such a manner.

In summary, the Office Action purports to combine three references that allegedly show each of the limitations of the claimed invention. While Applicant does not agree that the references (even if they could be combined) show each of the limitations in the claims, the references simply cannot be combined for any of the reasons described in the foregoing. Accordingly, the Office Action fails to establish a *prima facie* case of obviousness and the rejection is therefore improper. Accordingly, Applicant respectfully requests that the rejection of claims 1, 2, 3 and 5 be withdrawn.

#### IV. Allowable Subject Matter

Applicant appreciates the Examiner's indication of allowable subject matter in claim 4. In response to this favorable indication, Applicant has rewritten claim 4 in independent form

incorporating all of the subject matter of base claim 1 and dependent claim 3. Accordingly, claim 4 is believed to be in allowable condition.

V. New Claims

New claims 6-16 have been added to further define Applicant's contribution to the art. Independent claim 6 recites a clipping device to protect a circuit from overvoltages, the clipping device comprising a first contact arranged for connection to the circuit, a second contact arranged for connection to a reference potential, and a semiconductor component coupled between the first and second contacts and adapted to break down when an overvoltage is applied to the first contact, wherein the clipping device exhibits a negative dynamic resistance after breakdown of the semiconductor component at least for currents in a range from 1 to 10 amperes.

Nowhere does Rault, Ishii or Williams disclose or suggest a clipping device that "exhibits a negative dynamic resistance after breakdown of the semiconductor component at least for currents in a range between 1 to 10 amperes," as recited in claim 6. Therefore, claim 6 patentably distinguishes over Rault, Ishii and Williams, either alone or in combination, and is in allowable condition.

Claims 7-16 depend from claim 6 and are allowable for at least the same reasons.

**CONCLUSION**

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below to discuss any outstanding issues relating to the allowability of the application.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

***Eric BERNIER and Robert PEZZANI***

By William R. McClellan

William R. McClellan, Reg. No. 29,409  
WOLF, GREENFIELD & SACKS, P.C.  
600 Atlantic Avenue  
Boston, MA 02210-2211  
Tel. no. (617) 720-3500  
Attorneys for Applicant

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